

PCI Express Gen 1/Gen 2 Phy IP Core

Description

The TRC5024CPA is a four lane Gen 1 and 2 PCI Express Physical layer (Phy) IP core, delivering high-speed serial data transmission over controlled impedance transmission media such as copper cable, PCB traces or fiber optics. The device offers support for 2.5/5.0 Gbps PCI Express which include spread spectrum clocking, beacon out of band signaling and de-emphasis support. TRC5024 operates on 1.0/1.8v supplies. The IP is capable of transmitting and receiving serial data at 2.5 Gbps and 5.0 Gbps per lane with excellent bit error rate performance.

Each transmit section of the TRC5024CPA contains a low-jitter clock synthesizer, a parallel to serial converter with built in PCS transmit functions, and a CMOS output driver with selectable de-emphasis for use in backplane applications.

Each receive section contains an input limiting amplifier with on-chip terminations and selectable equalization levels, clock/data recovery PLL, and PCS receive functions. Built-in serial and parallel loopback modes. PRBS generator/checker and error detectors aid in support of testing.

The TRC5024CPA requires no external components for its clock synthesizers and clock recovery PLL. Three external resistors are needed to set the proper bias currents for its on-chip terminations.

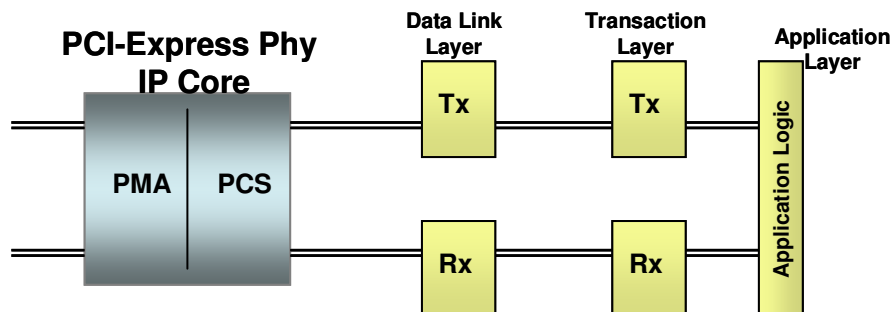
TRC5024CPA has low jitter generation and high jitter tolerance making it ideal for integration in SoCs and ASICs in the presence of multiple clocks and noise.

Features

- 2.5/5.0 Gbps per lane interface optimized for PCI Express applications
- PIPE compliant parallel interface
- Beacon out of band signaling
- Rate negotiation
- Receiver detection sequence
- High-speed differential reference clock
- Jitter Tolerance and Jitter generation exceeds the PCI Express Phy spec.
- Programmable output swing and de-emphasis
- Programmable serial input equalization
- Optional 1.5 v HSTL or 1.8 v SSTL I/O interface
- On-chip 8b/10b encoders and decoders
- Termination auto calibration on power up
- High speed serial CMOS output drivers with internal terminations
- High speed serial CMOS input stage with internal terminations
- On-chip synchronization for character alignment
- On-chip serial and parallel loopbacks
- On-chip Pseudo-Random (PRBS) pattern generator and error checker to support BIST
- Transmitter electrical idle, and receiver electrical idle detection
- 1.0/1.8V ±5% supplies
- Low Power: 125 mW/lane
- power management modes
- Available in TSMC advanced 90 nm and 65 nm CMOS process
- Small core size: Less than 0.5 mm²
- Portable to other processes
- PCI Express Gen 2 base specification rev 0.7 and PIPE1 version 1.86 compatible
- Available in 1X, 4X, 8X, and 16X configuration

Applications

- | | |
|------------------------|-------------------------|
| PCI Express Host | PCI Express End Point |
| Serial ATA Bridge | Infiniband Bridge |
| PCI Express Switch | PCI Express Add-in Card |
| PCI-PCI Express Bridge | ON chipset |



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Figure 2. Functional block diagram

