

10 Gbps XAUI SerDes IP Core

Description

TRC3114CBA is a Quad serializer/deserializer (SerDes) transceiver device IP core, delivering high-speed serial data transmission over controlled impedance transmission media such as copper cable, PCB traces or fiber optics. The device offers 10 Gbps XAUI compliant interface or alternatively four independent channels supporting 3.125 Gbps each. TRC3114CBA operates on 1.0/1.8 V supplies. The device is capable of transmitting and receiving serial data at 1.0625/2.125Gbps, 1.25/2.5Gbps, 2.125Gbps/2.25Gbps, or 1.562/3.125Gb/s per channel.

Each transmit section of the TRC3114CBA contains a low-jitter clock synthesizer, a parallel to serial converter with built in 8b/10b encoder, and a CML output driver with selectable pre-emphasis for use in backplane applications.

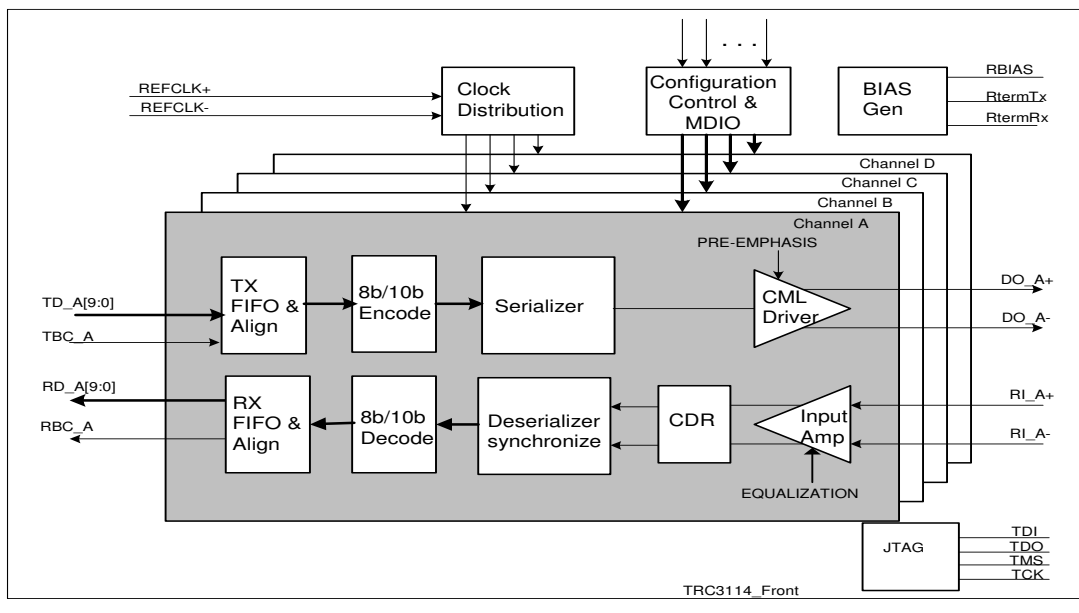
Each receive section contains an input limiting amplifier with on-chip terminations and selectable equalization levels, clock/data recovery PLL, Comma detector, and a serial to parallel converter with built-in 8b/10b decoder. A built-in serial loopback mode, PRBS generator/checker and error detectors aid in support of testing.

The TRC3114CBA requires no external components for its clock synthesizers and clock recovery PLLs. Three external resistors are needed to set the proper bias currents for the terminations.

Features

- 10 Gbps XAUI interface optimized for backplane applications
- Alternate independent 4x3.125 Gbps SerDes
- Per channel rates from 1.0625 to 3.125 Gbps
- Supports data rates from 1.0625 to 3.125Gb/s
- Jitter tolerance and jitter generation exceed specification
- High-speed differential reference clock
- Low jitter clock synthesizers for clock distribution
- 8b/10b encoder and decoder
- High speed serial CML output drivers with internal 50 Ω terminations
- High speed serial CML input stage with internal 50 Ω terminations
- Auto-calibration termination
- Supports up to four levels of pre-emphasis and equalization
- Synchronization for character alignment
- Comma Detect for character alignment
- Local serial loopback test mode
- Pseudo-Random (PRBS) pattern generator and error checker to support BIST
- Serial interface MDIO Clause 22
- 1149.1 compatible JTAG port
- 1.0/1.8V ±5% supplies
- Power dissipation: 100 mW/Ch
- TSMC advanced 90, 65 nm CMOS process

Figure 1. Functional block diagram



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Figure 2. Detail Functional block diagram

