

GPON ONU SerDes IP Core

Description

TRC2441CGA is a single Giga bit per second Passive Optical Network (GPON) ONU serializer/deserializer (SerDes) IP core, delivering high-speed serial data transmission over controlled impedance transmission media such as copper cable, PCB traces or fiber optics. The device offers a downstream data rate of 2.488 Gbps, 1.244 Gbps, and upstream data rate of 1.244 Gbps, 622 Mbps, and 155 Mbps and is ITU GPON (G.984.2) compliant interface. TRC2441CGA operates 1.0/1.8 V supplies. The device is capable of transmitting and receiving asymmetrical serial data up to 2.5 Gbps.

The transmit section of TRC2441CGA contains a low-jitter clock synthesizer derived from the receive clock data recovery block, a parallel to serial converter with built in PCS transmit functions, and a CML output driver with selectable pre-emphasis for use in Optical Network Unit (ONU) equipment and other GPON applications.

The receive section contains an input limiting amplifier with on-chip terminations and four (4) selectable equalization levels, clock/data recovery PLL using recovered clock from serial input data, and PCS receive functions. Built-in serial loop-back modes, IEEE 1149.1 compliant (JTAG) interface, PRBS generator/checker and error detector aid in support of testing and debugging.

TRC2441CGA requires no external components for its clock synthesizer and clock recovery PLL. TRC2441CGA's high jitter tolerance is ideal for use in SoCs and ASICs in the presence of multiple clocks and noise.

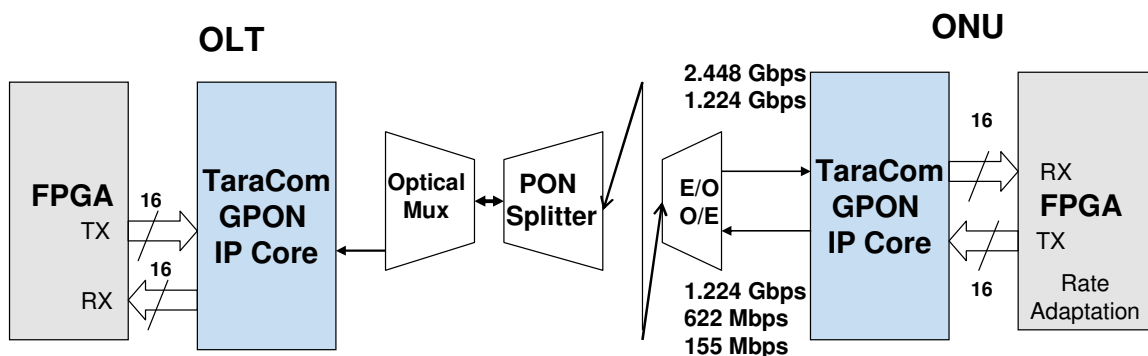
Features

- ITU GPON ONU Phy compliant (G.984.2)
- Downstream speed: 2.488Gbps/1.244Gbps data rate
- Upstream speed: 1.244Gbps/622Mbps/155Mbps data rate
- High-speed differential reference clock
- Jitter Tolerance and Jitter Generation exceed standard specification
- Supports Burst Mode
- Scrambler/Descrambler
- High-speed serial CML output drivers with internal 50 Ω terminations
- input stage with internal 50 Ω terminations
- Termination resistor calibration
- Supports up to four levels of pre-emphasis on the serial output drivers
- Supports up to four levels of equalization at the serial inputs
- Synchronization for character alignment
- Serial and parallel loop-backs
- 8b or 16b parallel interface
- Pseudo-Random (PRBS) pattern generator and error checker to support BIST
- Serial MDIO Clause 22 & 45
- 1149.1 compatible JTAG port
- Supply Voltage: 1.0 V/1.8V \pm 5%
- Power dissipation: 100 mW
- TSMC advanced 90 nm G/G OD CMOS process
- Portable to other processes

Applications

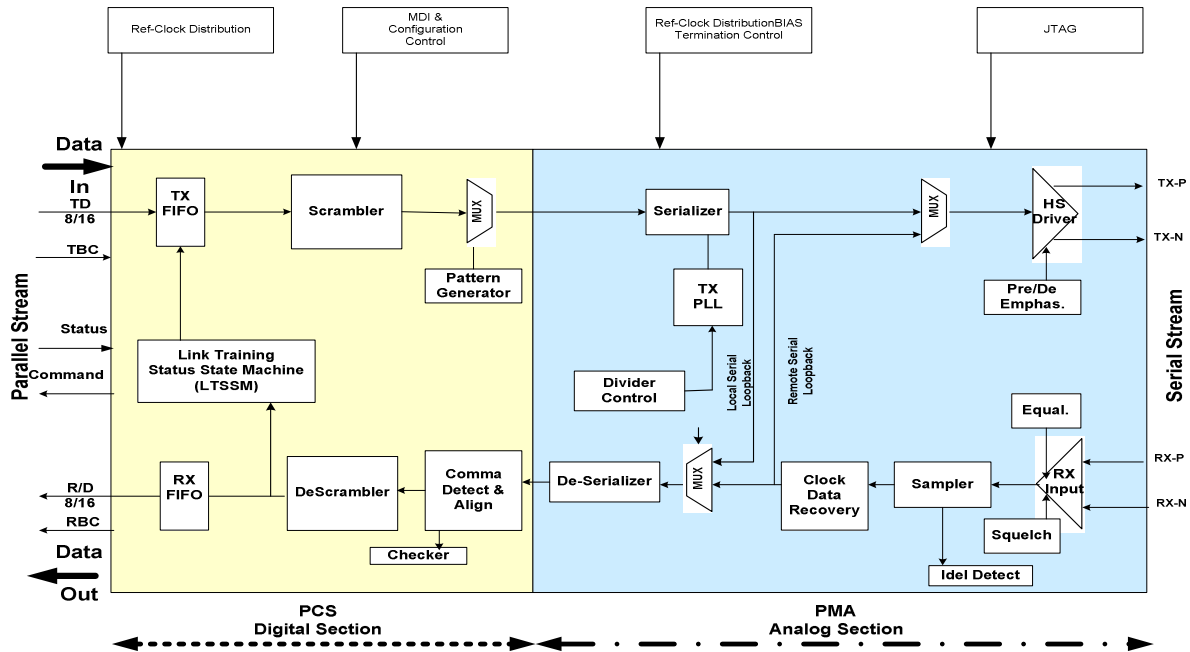
Gigabit Passive Optical Networks – GPON
WDM Transponders
Test Equipment

Figure 1: System Application



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Figure 2. Functional block diagram



General Description

TRC2441CGA consists of transmit and receive paths. Serial data arrives at the input receiver amplifier, after amplification it passes through an equalizer and a slicer. The analog input data is monitored in amplitude to indicate the loss of signal (LOS). The output of the slicer is used by the clock data recovery (CDR) to extract the clock and realign the data

A frequency locked loop is used to lock to the incoming data to determine the received data carrier frequency then a phase locked loop acquire phase lock and track the received data. A lock indicator circuit is used to indicate that CDR PLL is tracking the incoming data. The serial data is converted to parallel data by the deserializer block.

The parallel data arrives at the descrambler and decoded into 8-bit or 1-bit parallel data stream on to ASIC or FPGA. The parallel data is also probed by a pattern checker, which is used in test mode to evaluate the channel and error rate. The recovered Rx clock is used by the transmitter phase

locked loop (TX-PLL) to generate the clock needed to serialize the TX data and align the TX data before the driver.

A special divider-select signal is generated by the CDR and can be also programmed by the serial interface to select the TX clock data rate.

On the transmit path, parallel data stream arrive at the encoder and scrambler blocks where parallel data signal scrambled and encoded. The encoded data signal arrives in the serializer block. The serial data signal is clocked and transmitted to the transmit data alignment block and are sent to the driver block and transmitted on the media through high-speed output block.

TRC2441CGA has a built-in-self-Test (BIST) to generate many different pseudo random bit stream (PRBS) patterns to test the transmitter and receiver blocks. TRC2441CGA has parallel and serial loop-backs for testing and debugging. The loop-backs allow local and remote system level testing. The MDIO block allows serial access to internal registers for configuring the block.