

SGMII SerDes IP Core

Description

TRC1251CSG is a Serial Giga bit Media Independent Interface (SGMII) IP core and provides a single lane 1.25Gbps data rate interface to MAC layer and consists of Physical Convergent Sublayer (PCS) and Physical Media Dependent (PMD). SGMII IP transmitter includes Rate-Adaptation, Transmit state-machine, Serializer and transmitter IO blocks. The Receiver consists of Sampler, Clock Data Recovery (CDR), high performance Phase-Lock Loop (PLL), Synchronization, Receive state-machine, and Rate adaptation blocks. The SGMII IP has a high performance rate auto-negotiation block to negotiate rates between transmitter and receiver. The SGMII core is an ideal solution for applications requiring to integrate SGMII port(s) without depending on a separate clock line to time the data transfer, where lowest power and pin counts needed.

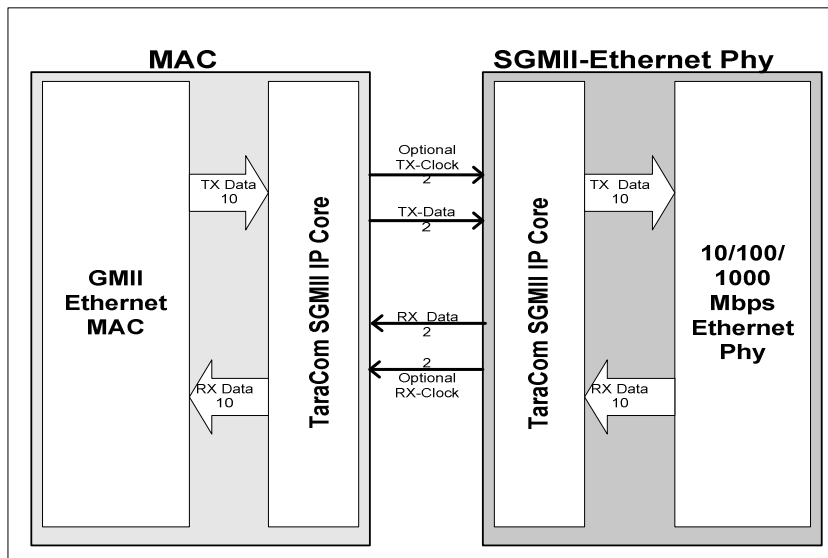
The transmit section of the TRC1251CSG contains a low-jitter clock synthesizer, a parallel to serial converter with built in 8b/10b encoder, and LVDS output driver with selectable pre-emphasis for use in backplane applications.

TRC1251CSG has a built-in serial loopback mode, PRBS generator/checker and error detectors aid in support of testing. TRC1251CSG requires no external components for its clock synthesizers and clock recovery PLLs. Three external resistors are needed to set the proper bias currents for its on-chip terminations.

Features

- Fully Compliant with Cisco revision 1.7 of Serial GMII Specification
- 1.25 Gbps Serial GMII interface
- Rate adaptation
- LVDS I/O
- High-speed differential reference clock
- Low jitter clock synthesizers for clock distribution
- Jitter performance exceeds SGMII spec.
- 8b/10b encoder and decoder
- Auto-calibration termination
- Supports up to four levels of pre-emphasis on the serial output drivers
- Supports up to four levels of equalization at the serial inputs
- Comma Detect for character alignment
- Local serial loopback test mode
- Pseudo-Random (PRBS) pattern generator and error checker to support BIST
- Serial interface MDIO
- Single 1.0/1.8 V $\pm 5\%$ supplies
- Low Power: 30 mW
- Power management
- TSMC advanced 90 and 65 nm CMOS process
- Portable to other processes

Figure 1. General Application Block Diagram



SGMII SerDes IP Core

Figure 2. Functional block diagram

